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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,222	12/04/2003	Jae-Bon Koo	6161.0114.US	4976

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EXAMINER	
LANDAU, MATTHEW C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/727,222	KOO ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 1 and 24-27 are objected to because of the following informalities:

Regarding claim 1, the limitation "a direction of current flow" occurring twice in the last paragraph of the claim should be changed to read "the direction of current flow", since the directions have already been identified in the previous paragraph.

Regarding claims 24-27, the degree symbol has either been omitted or replaced with a parenthesis.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-3 are rejected under 35 U.S.C. 102(a) as being anticipated by Yamazaki et al. (US PGPub 2003/0062845, hereinafter Yamazaki).

Regarding claim 1, Figures 1, 2, and 5 of Yamazaki disclose a light emitting device 121; a switching thin film transistor 101 including a semiconductor active layer 110 having at least a channel area for transferring a data signal to the light emitting device; and a driving thin film transistor 102b including a semiconductor active layer 111 having at least a channel area for driving the light emitting device so that a predetermined current flows through the light emitting

device according to the data signal, wherein with respect to a direction of any grain boundary, the channel area of the switching transistor is situated along a first direction and the channel are of the driving transistor is situated along a second direction, and wherein a direction of current flow in the channel area of the switching thin film transistor is different from (not the same as) a direction of current flow in the channel area of the driving thin film transistor with respect to any grain boundary. Figures 15A to 15E of Yamazaki show examples of devices using the display disclosed by Yamazaki. All of these devices have flat panel displays, which inherently comprise a plurality of pixels. It is inherent that the channel of the switching transistor 101 has a grain boundary. Figures 1 and 5 of Yamazaki show that the channel direction (i.e., direction of current flow) in the switching transistor 101 is perpendicular to the channel direction (direction of current flow) in the driving transistor 102b. Therefore, it can be considered the channel area of the switching transistor is situated along a first direction with respect to the grain boundary and the channel area of the driving transistor is situated along a second direction with respect to the grain boundary, wherein the first direction is different from (not the same as) the second direction.

Regarding claims 2 and 3, Figure 5 of Yamazaki disclose the crystal growth direction is parallel to the channel of the switching transistor 101 and perpendicular to the channel of the driving transistor 102b, and that the current mobility of the switching transistor will be greater than that of the driving transistor (page 4, paragraph [0048] and Table 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Komiya et al. (US Pat. 6,456,013, hereinafter Komiya).

Regarding claim 4, Yamazaki discloses the active layer is formed from polycrystalline semiconductor material (page 4, paragraph [0052]), but does not specifically disclose using polycrystalline silicon. Figure 3 of Komiya discloses a display device using a polycrystalline silicon active layer 13 (col. 5, lines 40-45). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Yamazaki by using polycrystalline silicon for the purpose of selecting an inexpensive semiconductor material that has high carrier mobility.

Regarding claims 5 and 18, Yamazaki discloses the polycrystalline semiconductor (silicon) has anisotropic crystal grains (page 4, paragraph [0053]).

Regarding claims 6 and 19, a further difference between Yamazaki and the claimed invention is a crystal grain has a first length which is at least 1.5 times longer than a second length in direction which is substantially perpendicular to a direction of the first length. It is inherent that crystal grains in the active layers (110 and 111) of Yamazaki have first and second lengths, and that the first length (in a direction parallel with crystal growth direction shown in

Figure 5) is longer than the second length (in a direction perpendicular to the crystal growth direction). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of by having the first length be at least 1.5 times longer than the second length, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 7 and 8, it is inherent that the grains in the active layers (110 and 111) of Yamazaki have longer grain boundaries that run parallel to the crystal growth direction (shown in Figure 5). Therefore, Figure 5 of Yamazaki disclose semiconductor (silicon) grains including longer grain boundaries situated along a direction which makes a first angle (approximately 0 degrees) with a direction of current flow in the channel are of the switching transistor 101 and a second angle (approximately 90 degrees) with a direction of current flow in the channel area of the driving transistor 102b. Note that the second angle is larger than the first angle.

Regarding claims 9 and 21, when using the laser beam solidification method disclosed by Yamazaki (paragraphs [0052]-[0059]), it is inherent that the polycrystalline semiconductor will have "primary" grain boundaries that are perpendicular to the direction of the "side" grain boundaries of the anisotropic grains, and that the average interval between the side grain boundaries is shorter than the average interval between adjacent primary grain boundaries.

Regarding claims 10, 11, 13, 15, 22, 23, 25, and 27, since the primary grain boundaries are perpendicular to the side grain boundaries (which extend in a direction corresponding to the length direction of the grains, which corresponds to the direction of crystal growth shown in

Figure 5), the direction of current flow in the channel area of the switching thin film transistor 101 makes a first angle (90 degrees) with a direction along which the primary grain boundaries are situated and the direction of current flow in the channel area of the driving thin film transistor makes a second angle (0 degrees) with the direction along which the primary grain boundaries are situated.

Regarding claims 12, 14, 24, and 26, since the side grain boundaries extend in a direction corresponding to the length direction of the grains, which corresponds to the direction of crystal growth shown in Figure 5 of Yamazaki, they form an angle of approximately 0 degrees with the direction of current flow in the channel area of the switching thin film transistor, and they form and angle of approximately 90 degrees with the direction of current flow in the channel area of the driving thin film transistor.

Regarding claims 16 and 20, Figures 1, 2, and 5 of Yamazaki disclose a light emitting device 121; a switching thin film transistor 101 which is formed using a polycrystalline semiconductor (page 4, paragraph [0052]) and includes a semiconductor layer 110 having a channel area for transferring a data signal to the light emitting device; and a driving thin film transistor 102b which is formed using a polycrystalline semiconductor and includes a semiconductor layer 111 having a channel area for driving the light emitting device so that a predetermined amount of current flows through the light emitting device, wherein the channel area of the switching thin film transistor has a first angle (approximately 0 degrees) between a length direction of polycrystalline semiconductor grains and a direction of current flow in the channel area and the channel area of the driving thin film transistor has a second angle (approximately 90 degrees) between a length direction of polycrystalline grains and a direction

of current flow in the channel area; and wherein the first angle is not the same as the second angle. Note that it is inherent that the length direction of the grains corresponds to the direction of crystal growth shown in Figure 5 of Yamazaki. Figures 15A to 15E of Yamazaki show examples of devices using the display disclosed by Yamazaki. All of these devices have flat panel displays, which inherently comprise a plurality of pixels. The difference between Yamazaki and the claimed invention is using polycrystalline silicon. Figure 3 of Komiya discloses a display device using a polycrystalline silicon active layer 13 (col. 5, lines 40-45). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Yamazaki by using polycrystalline silicon for the purpose of selecting an inexpensive semiconductor material that has high carrier mobility.

Regarding claim 17, the second angle (indicated above as being approximately 90 degrees) could also be considered –90 degrees. This would mean that the first angle (indicated above as being 0 degrees) is larger than the second angle.

Response to Arguments

Applicant's arguments filed June 16, 2005 have been fully considered but they are not persuasive.

In response to applicant's argument regarding claim 1 that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., having only one driving TFT at each pixel) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification

are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The claim does not in any way state that each pixel can have only one driving TFT. As noted by Applicant, and as stated in the above rejection, Yamazaki discloses a driving transistor (102b) that has a direction different from that of the switching TFT. The claim as written does not exclude having another driving TFT with a direction the same as that of the switching TFT. Therefore, claim 1 is fully anticipated. Applicant makes similar arguments regarding claim 16.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER

Matthew C. Landau

August 25, 2005